Communication and Networking Riser (CNR) System

Design Guide

Version 1.1

January 2001

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Revision History

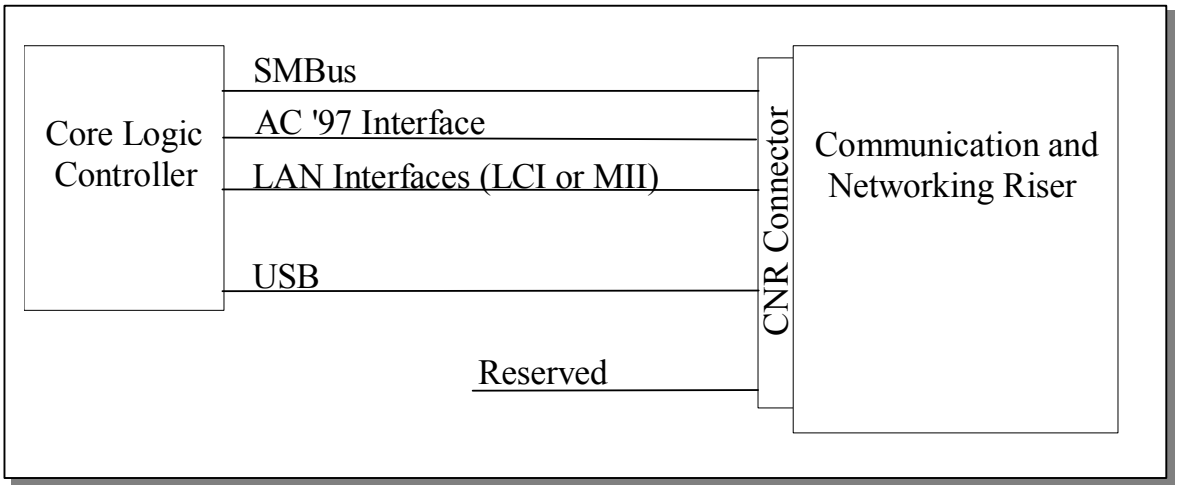
Rev.	Description	Date
1.0	• Initial Release	August 2000
1.1	• New addition of USB2.0 routing section	January 2001

1. Introduction

1.1. Scope

A primary function of this document is to provide a single resource, containing much of the essential information, required to implement robust Communication and Networking Riser (CNR) designs. CNR design-related information is covered in a number of industry-standard or Intel proprietary interface specifications and implementation documents. This guide is not intended to replace these original source documents, but rather to centralize the information and expand on it. The intended audience for this document consists of CNR card manufacturers and motherboard manufacturers implementing the CNR interface.

Figure 1-1. Generic CNR Subsystem



CNR supports four interfaces (Figure 1-1)

Figure 0System Management Bus (SMBus); provides Plug and Play (PnP) system configuration capability

Figure 1Audio codec ’97 (AC ’97); provides audio and v.90 modem capability

Figure 2Local Area Network (LAN) Interfaces (LCI or MII)

Example LAN Connect Interface (LCI); CNR Connector Type A pin-out; provides support for Ethernet, Local Area Network (LAN), and Home Phone Network Alliance (HPNA) capability

Example AMedia Independent Interface (MII); CNR Connector Type B pin-out; provides support for LAN and HomePNA capability that may be integrated into non-Intel chipsets

Figure 3Universal Serial Bus (USB); provides added USB I/O ports or high-speed communications capability

1.2. Benefits of CNR

By using a CNR solution, a system designer can use one or more of the interfaces listed above to tap directly into the integrated functions of a core logic chipset (i.e., Ethernet MAC, AC '97 digital controller, USB controller). CNR is an OEM or system integrator implementation; it allows developers to hit a price point between motherboard integration and PCI (or other standard/proprietary bus implementations). CNR provides the general benefits of developer flexibility, lower cost, and reduced Time To Market (TTM).

CNR achieves these benefits in the following ways:

Figure 4 Reduces cost of add-in Printed Circuit Boards (PCB)s (a CNR card has a smaller minimum PCB size and interface connector)

Figure 5 Eliminates cost of PCI bridge inherent in all PCI card designs (with CNR, the chipset drives the function directly to the CNR device)

Figure 6 Provides better noise immunity and signal quality (because of the physical separation of I/O circuitry from motherboard circuitry)

Figure 7 Potential to reduce need to perform FCC and/or other international communication certifications (Homologation) on motherboards (CNR cards may be certified and then used across multiple motherboards)

Figure 8 Supports system integrators using a single motherboard across multiple system models (using CNR to add the differentiating features)

Figure 9 Provides a variety of branded audio and/or v.90 modem solutions using a single motherboard

1.3. CNR vs. AMR

CNR is not simply an evolution of the Audio Modem Riser (AMR); instead, it replaces the AMR. Because of three key reasons, CNR was designed **not** to be backward compatible:

Figure 10 **Losing a PCI slot:** Motherboard designers implementing the AMR connector were not able to share the slot with the adjacent PCI connector. If the design carried the footprint for AMR, a PCI slot was lost, even on product variations that did not populate the AMR connector.

Figure 11 **Lack of Plug and Play:** AMR did not implement an acceptable PnP methodology. Non-PnP I/O interfaces tend to generate high customer service call rates. AMR can also be problematic for OEMs or system integrators doing Windows† Hardware Quality Lab (WHQL) testing.

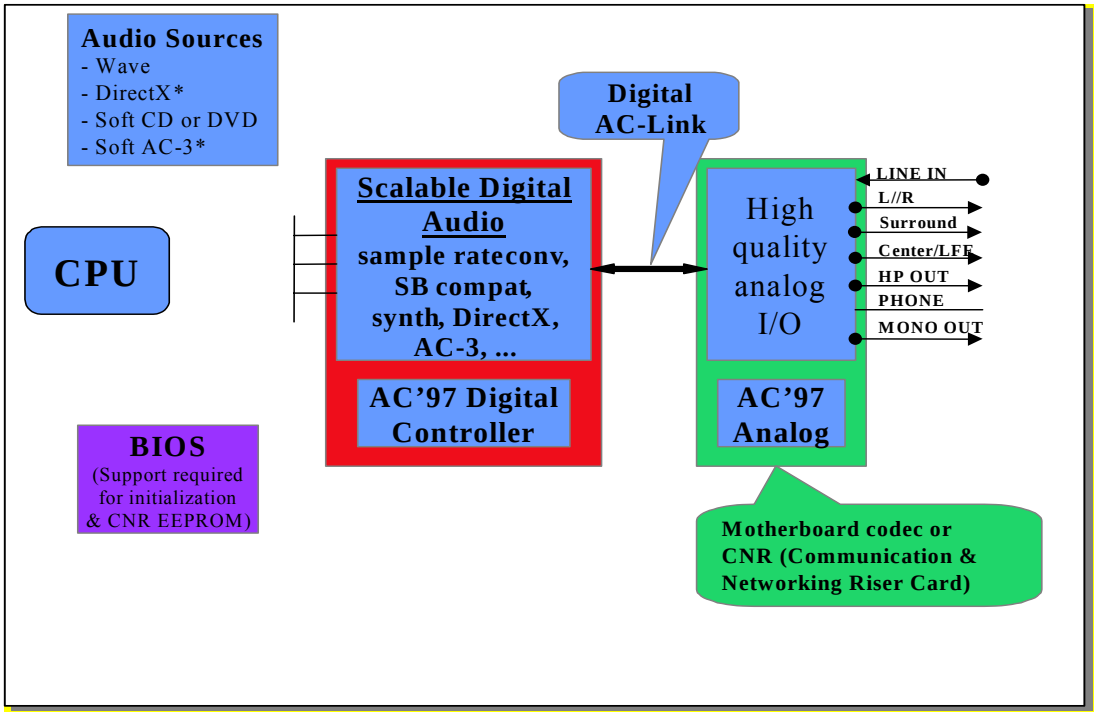
Figure 12 **Insufficient pins for new interfaces:** To add LAN capability and SMBus for PnP, several additional pins were required.

Considering the above, it was determined that CNR could best resolve old AMR issues if backward compatibility was not maintained.

2. AC '97 Codec Management

The AC '97 interface on CNR can support two AC '97 codecs (Figure 2-1) The codecs can be audio, v.90 modem, and/or audio/v.90 modem, and they can be partitioned onto the motherboard, the CNR card, or both. There is significant complexity in determining which codecs perform which functions. All AC '97 codecs in the system must be managed dynamically. This section details the design requirements for both motherboards and CNR cards in respect to dynamic codec management.

Figure 2-1. AC '97 Overview



2.1. Codec Down Enable (CDC_DN_ENAB#)

Implementing the complete functionality of the CDC_DN_ENAB# signal requires support of the *AC '97 codec Disable and Demotion Rules*. Also, there is circuitry required on both the motherboard and on the CNR card. The motherboard and the CNR card *must* implement each of these requirements to allow interoperability.

2.1.1. AC '97 Codec Disable and Demotion Rules

To help manage codec configuration complexities, several rules were developed. These can be divided into two classes, one for the motherboard-based AC '97 codecs and another for the CNR-based AC '97 codecs.

Motherboard-based AC ’97 codec Disable and Demotion Rules:

1. All AC ’97 codecs on the motherboard should always disable themselves when the CDC_DN_ENAB# signal is in a high (inactive) state.
2. A motherboard AC ’97 codec should *never* change its address or SDATA_IN line, regardless of the state of the CDC_DN_ENAB# signal. Only the CNR based codec is demoted. The address of a motherboard codec and the SDATA_IN line it uses *must* stay fixed.
3. A motherboard with two AC ’97 codecs on the same AC ’97 Interface should implement circuitry (on the motherboard) to disable any codec appearing on CNR.

The following three circuit diagrams show examples of how CDC_DN_ENAB# and AC97_RESET# are used to ensure that no more than two codecs are present, at any given time, on the AC ’97 interface. Other possible configurations exist, and in these cases, designers must implement circuitry to comply with the codec Disable and Demotion Rules. (See Figure 2-2, Figure 2-3 and Figure 2-4.)

Figure 2-2. Two CNR codecs Cause Motherboard codec to Be Held in Reset

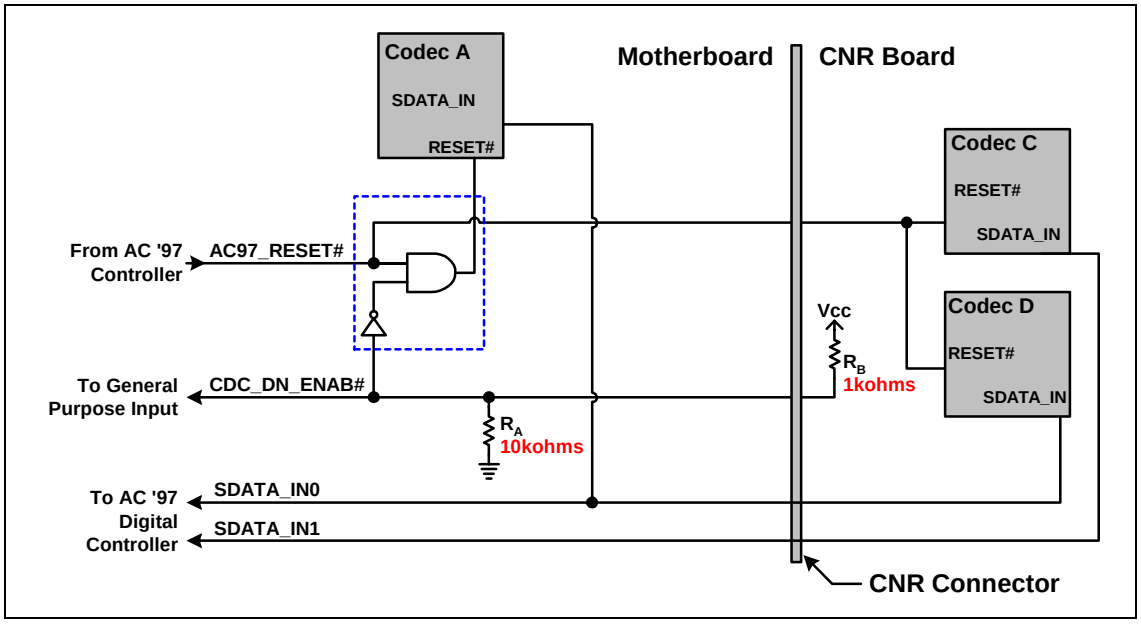


Figure 2-3. Primary codec on Motherboard Causes CNR codec to Demote to Secondary

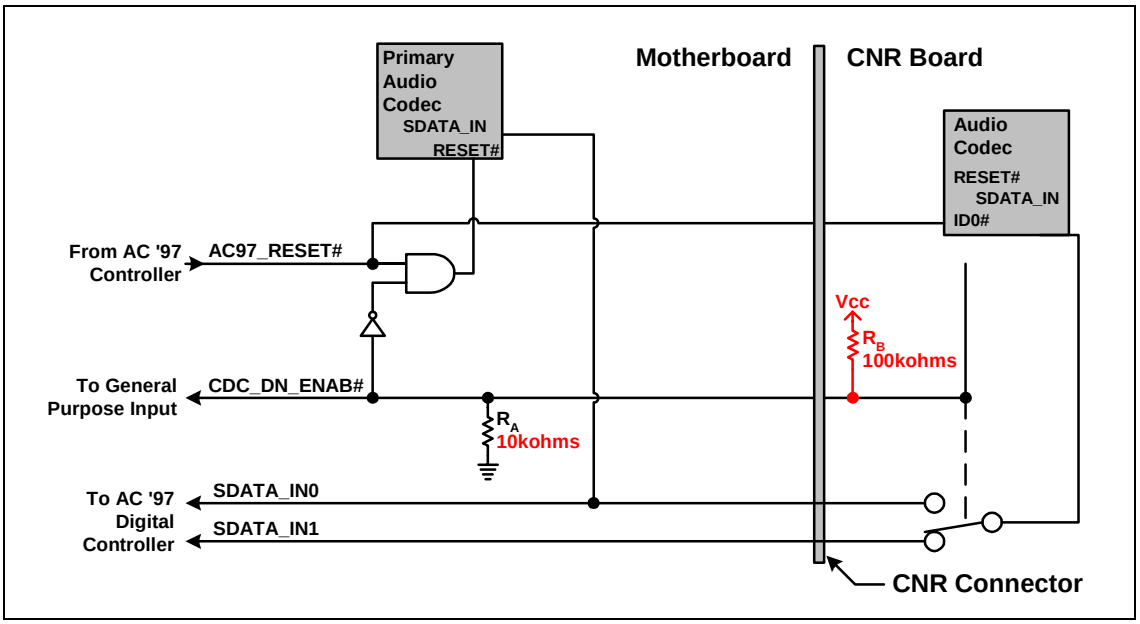
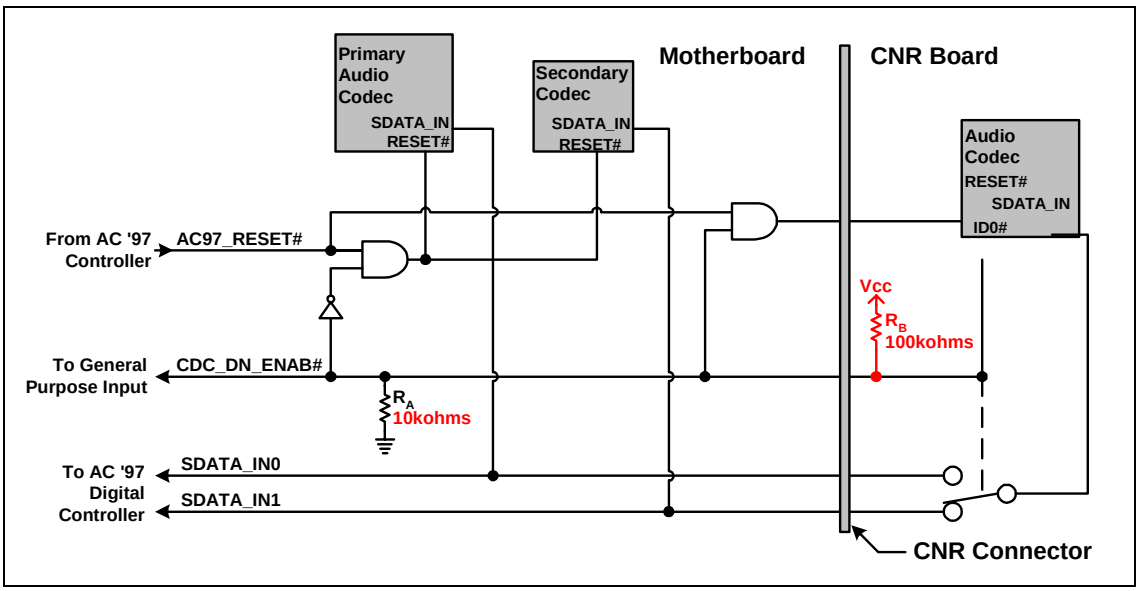


Figure 2-4. Two Codecs on Motherboard Cause CNR codec to Be Held in Reset

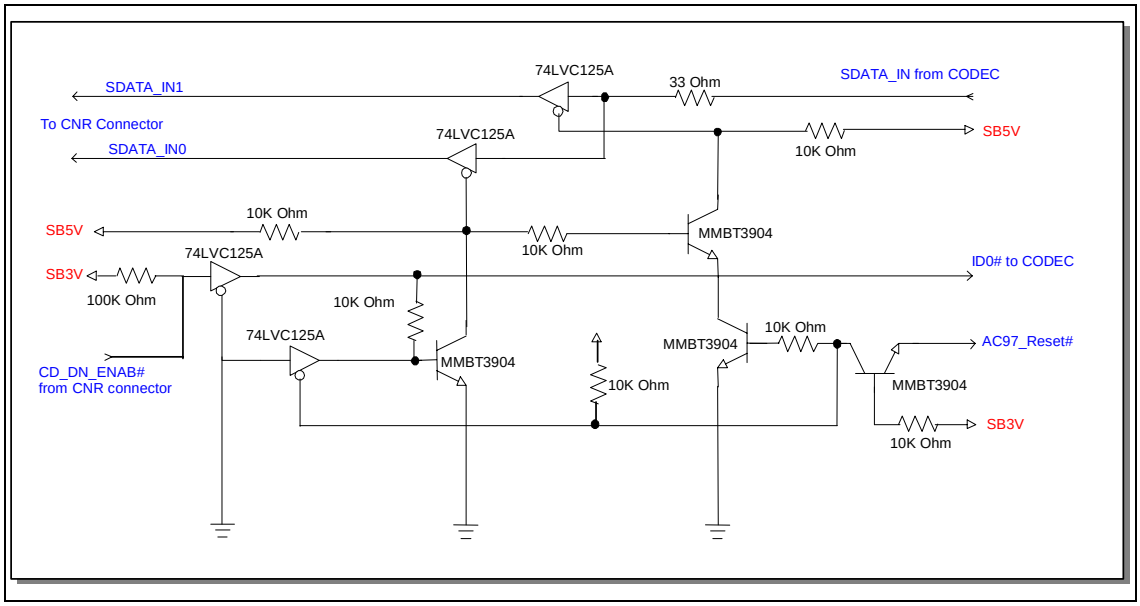


CNR-based AC ’97 codec Disable and Demotion Rules:

1. A CNR with a single AC ’97 codec *must* always demote itself to the next available address on the AC’97 Interface and switch to the next available SDATA_IN signal when the CDC_DN_ENAB# signal is in an active low state. If CDC_DN_ENAB# is asserted, then SDATA_IN0 is in use and the CNR cannot use SDATA_IN0.
2. A CNR AC ’97 codec *must never* change its address or SDATA_IN line when the CDC_DN_ENAB# signal is in an inactive or high state.

Switching of SDATA_IN0 to SDATA_IN1 should be done through electrical means or through a manufacturing stuffing option. Jumpers should not be used on production-level CNR cards or reference designs. The circuit in Figure 2-5 implements the required switching between SDATA_IN0 and SDATA_IN1. This circuit can be used in cases where the desired codec does not support changing the SDATA_Inx line it uses.

Figure 2-5. Dynamic Switching of SDATA_IN0 and SDATA_IN1



3. Multichannel AC '97 Audio

Intel's first-generation integrated AC '97 Controller (referred to hereafter as Intel ICH or I/O Controller Hub) was designed to support dual codecs (one Audio codec and one V.90 modem codec). Intel's second-generation integrated AC '97 Controller (referred to hereafter as Intel ICH2) maintains dual codec support but adds split codec support for multichannel (2, 4, 6) audio and Sony/Philips Digital Interface (S/PDIF*) output capability.

Note: *For Intel ICH designs the phrase dual codecs referred to a pair comprised of one audio codec and one modem codec. Intel ICH2 supports the splitting of audio functions across two codecs, hence the phrase split codecs*

Intel originally envisioned a single, monolithic codec providing all audio functionality, with motherboard audio as the predominant implementation, and limited use of riser cards as vehicles for enhancing OEM and system integrator configurations. Following this vision, motherboards with audio populated would not be upgradable, and motherboards without audio would offer 2-, 4-, or 6-channel audio with or without S/PDIF* via riser (or PCI) add-in card audio only.

With CNR, and PnP functionality, it becomes feasible to consider motherboard audio augmented with a second (split) codec on a riser—enabling the potential for point-of-sale motherboard audio upgrades via addition of a riser card.

3.1. AC '97 Codec Types

Table 3-1 lists possible audio codec types that will be referred to throughout this discussion. The type numbers are arbitrary (assigned for identification purposes only) and do not correspond to any bit fields in the AC '97 or CNR specifications.

Table 3-1. Multichannel Audio Configuration Types

Type	Function	AC '97 Slot numbers			
		3&4	7&8	6&9	10&11*
00	2-ch Primary	L&R	—	—	—
01	2-ch Primary with S/PDIF*	L&R	S/PDIF*	—	—
02	4-ch Primary	L&R	Surround	—	—
03	4-ch Primary with S/PDIF*	L&R	Surround	S/PDIF*	—
04	6-ch Primary	L&R	Surround	C/LFE	—
05	6-ch Primary with S/PDIF*	L&R	Surround	C/LFE	S/PDIF*
06	+2-ch Surround	—	Surround	—	—
07	+2-ch Surround with S/PDIF*	—	Surround	S/PDIF*	—
08	+4-ch Surround/Center/LFE	—	Surround	C/LFE	—
09	+4-ch Surround/Center/LFE with S/PDIF*	—	Surround	C/LFE	S/PDIF*
10	+2-ch Center/LFE	—	—	C/LFE	—

Type	Function	AC '97 Slot numbers			
		3&4	7&8	6&9	10&11*
11	+2-ch Center/LFE with S/PDIF	—	—	C/LFE	S/PDIF

— Slots 10&11 were originally allocated to v.90 modem line 2 and handset but are available when no v.90 modem codec is used (or when a combination audio/v.90 modem codec does not support line 2 and handset). Dedicated support for S/PDIF on slots 10&11 is not supported by the Intel ICH and Intel ICH2.

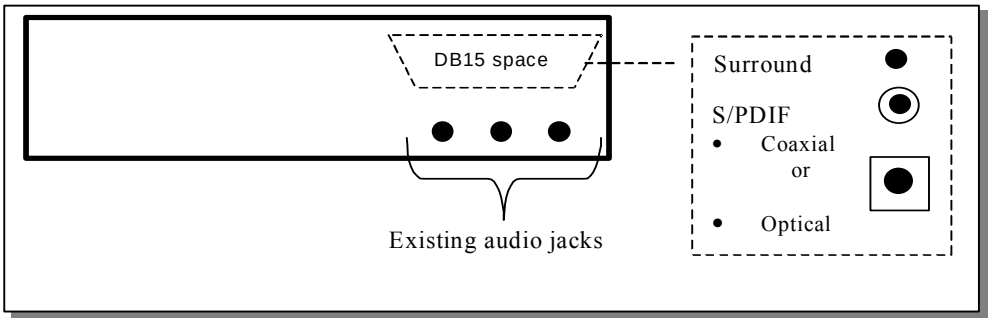
3.2. Recommendations for Motherboard Audio

The following motherboard audio solutions (highlighted in bold in the tables below) are recommended:

1. **Basic motherboard audio:** 2-channel (upgradable via CNR, see Section 3.4)
2. **Mainstream motherboard audio:** 4-channel (vendor-specific CNR, upgrade-feasible but not very compelling)
3. **Audiophile motherboard audio:** 2- or 4-channel with S/PDIF* (not upgradable via CNR)

To support motherboard 4-channel and/or S/PDIF*, Intel suggests using a revised back panel connector that eliminates the stacked DB15 game-port/MIDI connector and replaces it with added stereo mini-jacks for Surround channel output and coaxial or optical S/PDIF* (Figure 3-1)

Figure 3-1. Multichannel Audio Back Panel Recommendation



3.2.1. Motherboard Audio Support

Intel ICH Support:

Intel's ICH supports 2-channel audio with S/PDIF, for codec types 00-01, configured as Primary (codec ID 00) on the motherboard. For Intel ICH, the audio solutions highlighted in bold in Table 3-2are recommended.

Table 3-2. Recommended First Generation (Intel ICH) Motherboard Audio Support

Intel ICH Support for Motherboard AC '97 Audio			
Type	Function	codec ID	AC '97 Slot Nos. 3 & 4
00	**2-ch Primary**	**00**	**L&R**
01*	2-ch Primary with S/PDIF	00	L&R, S/PDIF

— Type 01 codec implementations have S/PDIF concurrency limitations. Dedicated support for S/PDIF* is not supported by Intel ICH.

Intel ICH2 Support:

Intel's ICH2 supports 2-, 4-, or 6-channel audio with concurrent S/PDIF, for codec types 00-05 configured as Primary (codec ID 00) on the motherboard. For ICH2, the audio solutions highlighted in bold in Table 3-3are recommended.

Table 3-3. Recommended Second Generation (ICH2) Motherboard Audio Support

Intel ICH2 Support for Motherboard AC '97 Audio					
			AC '97 Slot Nos.		
Type	Function	codec ID	3&4	7&8	6&9
00	2-ch Primary	00	L&R	—	—
01	**2-ch Primary with S/PDIF**	**00**	**L&R**	**S/PDIF**	**—**
02	**4-ch Primary**	**00**	**L&R**	**Surround**	**—**
03	**4-ch Primary with S/PDIF**	**00**	**L&R**	**Surround**	**S/PDIF**
04	6-ch Primary	00	L&R	Surround	C/LFE
05*	6-ch Primary with S/PDIF	00	L&R, S/PDIF	Surround	C/LFE, S/PDIF

—

— Type 05 codec implementations have S/PDIF concurrency limitations. Dedicated support for S/PDIF on slots 10&11 is not supported by the ICH2.

— The market infrastructure for 6-channel analog audio (content, applications, OS, speakers, etc.) was limited at the time this version (1.0) was published.

3.3. Recommendations for Primary CNR Audio

CNR audio enhances flexibility for configurations where no audio resides on the motherboard.

Intel recommends the following Primary CNR audio solutions

1. **Basic CNR audio:** Primary 2-channel audio for value systems
2. **Audiophile CNR audio:** Primary 2- or 4-channel audio codec with S/PDIF, high-quality Digital to Analog Converters (DACs), and gold connectors

3.4. Guidelines for Motherboard plus Secondary CNR Audio Upgrades

The most compelling audio upgrade uses a stereo system (i.e., 2-channel motherboard audio) and adds multichannel capability-support for Surround channels (4-speaker output) and S/PDIF output (digital AC-3† 5.1 export).

Intel recommends just one motherboard plus CNR audio upgrade solution for mainstream desktop PCs.

1. Basic-to-audiophile 2-channel on motherboard +2 Surround with S/PDIF* on CNR: Add Secondary 2-channel audio codec with S/PDIF*.

Intel's current recommendation for motherboard plus CNR audio upgrades is that the same codec vendor should provide both motherboard codec and riser codec. The OEM and system integrators should insure that both the motherboard and the CNR codecs are of the same family from a single vendor.

(See white paper, *Intel Recommendations for ICHx/AC '97 Audio*, for additional details about multichannel audio implementations.)

4. LAN and HPNA

A principal interface of CNR is the LAN Connect Interface (LCI). There are two possible LAN implementations using the interface. One is the Media Independent Interface (MII). This document will not address MII until a later revision. The other implementation is a reduced pin-count LAN interface (sometimes referred to as the Jordan Interface).

Note: Implementation of the two LAN interfaces (LCI and MII) on CNR is mutually exclusive. These guidelines use the 82562ET to refer to both the 82562ET and the 82562EM. The 82562EM is specified in those cases where guidelines are different between the two components.

4.1. Bus Topologies and Line Lengths

The LAN Connect Interface is best configured using one of the following topologies:

Figure 13Direct point-to-point connection between the Intel ICH2 and the LAN component

Figure 14LAN On Motherboard (LOM)/CNR Implementation

4.1.1. Point-to-Point Interconnect

Figure 4-1and the table provide guidelines for a single-solution motherboard. Either 82562EM, 82562EH, 82562ET, or CNR is installed.

Figure 4-1. Single Solution Interconnect

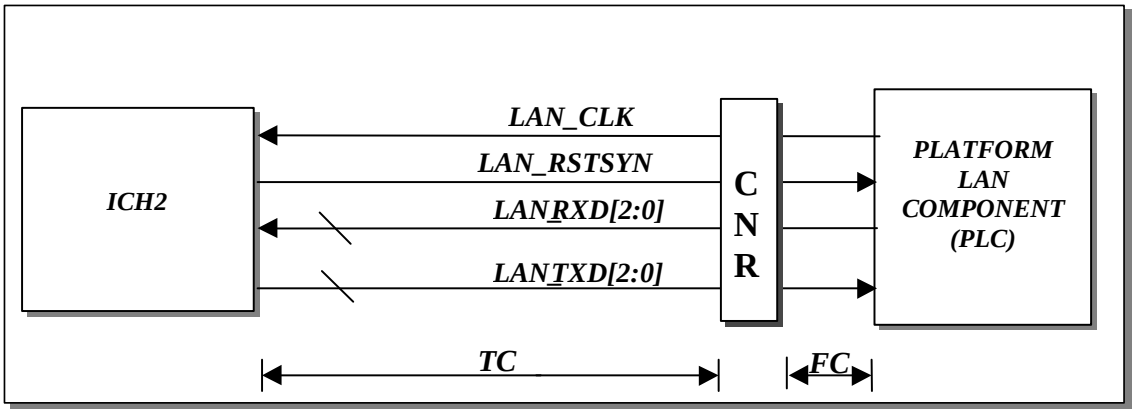


Table 4-1. Trace length requirements

Configuration	Length
82562EH	L = 4.5” to 10”
82562ET	L = 3.5” to 9.5”
82562EM	L = 3.5” to 9.5”
CNR	TC = 3” to 9”
CNR	FC = 0.5” to 3”

4.1.2. Networking on Motherboard or on CNR

Figure 4-2 and the table provide guidelines for an all-inclusive motherboard solution. The layout combines a motherboard site for either an Ethernet LAN or HPNA PLC device ***or*** either solution on a CNR card. The resistor pack ensures that only one of the options is implemented at one time. The recommended trace routing lengths are shown below.

Figure 4-2. Optional Motherboard or CNR PLC Interconnect

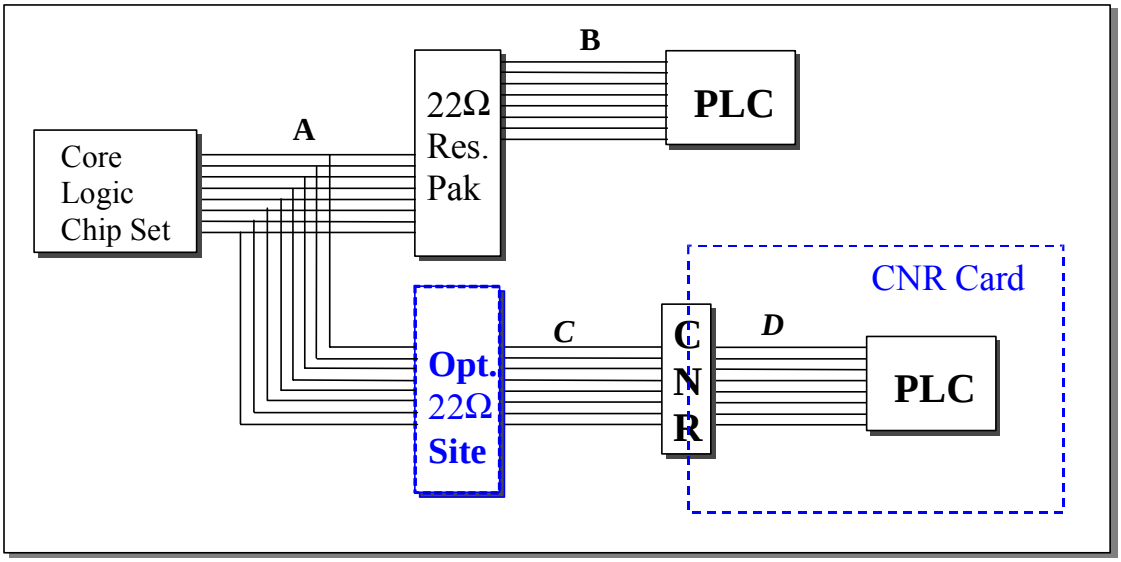


Table 4-2. Trace length requirements

Configuration	A	B	C	D
82562EH	0.5” to 6”	4” to (10”-A)		
82562ET	0.5” to 7”	3” to (10”-A)		
Dual Footprint	0.5” to 6.5”	3.5” to (10”-A)		
82562ET/EH Card*	0.5” to 6.5”		2.5” to (9” – A)	0.5” to 3”

— * Total trace length should not exceed 12 inches

Additional guidelines for motherboard/CNR configuration:

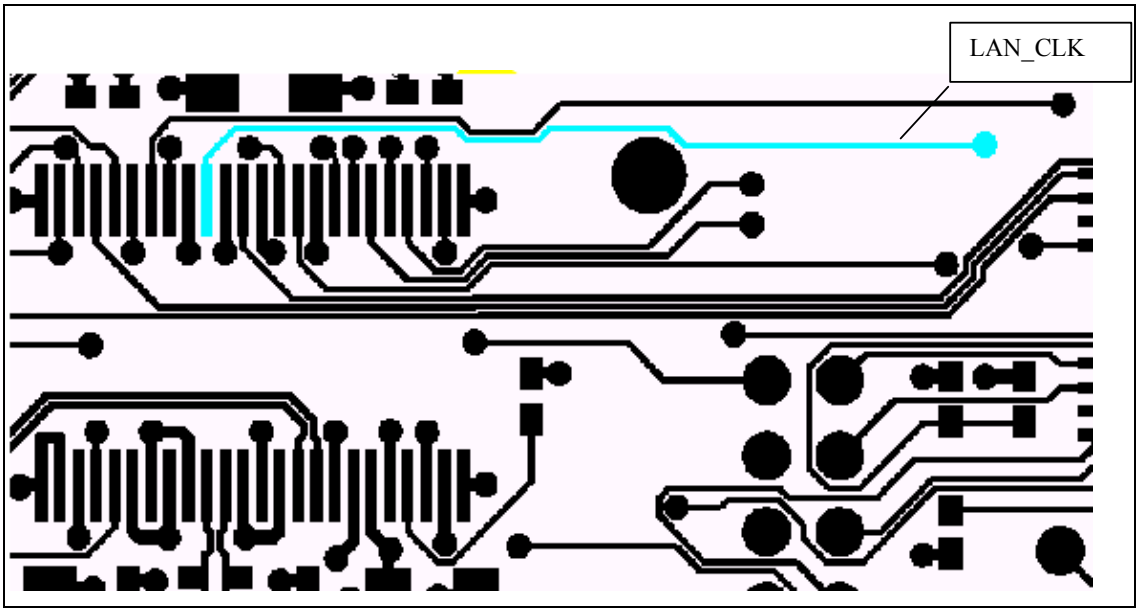
Figure 15 The resistor value should be 22Ω.

Figure 16LAN on motherboard PLC can be a dual-footprint configuration. This would allow a single motherboard to support either the Ethernet LAN device or the HPNA device.

4.2. Routing and Signal Layout Guidelines

LAN Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of the applicable Intel ICH specification. This section describes general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and cross-talk. On the motherboard, the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.) Figure 4-3 shows an example.

Figure 4-3. LAN_CLK Routing Example



4.2.1. Cross-talk Consideration

Noise caused by cross-talk must be carefully controlled to a minimum. Cross-talk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter.

4.2.2. Impedances

The motherboard impedances must be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω +/-15% is strongly recommended; otherwise, signal integrity requirements may be violated.

4.2.3. Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ring-back. A 33Ω series resistor can be installed at the driver side of the interface if the developer has concerns about over/undershoot. The receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

4.3. General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of cross-talk and propagation delays on sections of the board where high speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

Figure 17Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inch.

Figure 18Maintain constant symmetry and spacing between the traces within a differential pair.

Figure 19Keep the signal trace lengths of a differential pair equal to each other.

Figure 20Keep the total length of each differential pair under 4 inches.

Note: Several designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE PHY conformance failures, excessive EMI, and/or degraded receive Bit Error Rate (BER).

Figure 21Do not route the transmit differential traces closer than 70 mils to the receive differential traces.

Figure 22Do not route any other signal traces both parallel to the differential traces, and closer than 70 mils to the differential traces.

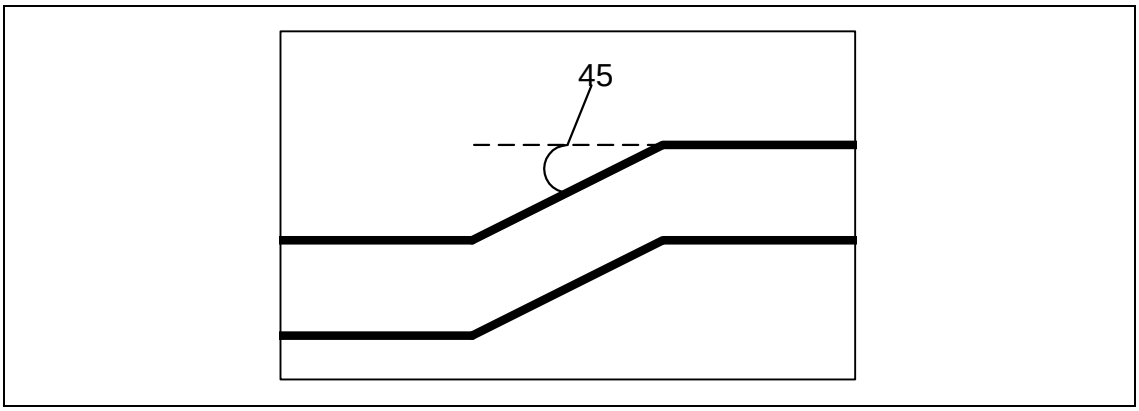
Figure 23Keep maximum separation between differential pairs to 7 mils.

Figure 24For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead (Figure 4-4).

Figure 25Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

Figure 26Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 4-4. High-speed Trace Routing



4.3.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, the ratio of trace width to height above the ground plane is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 ohms. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 ohms, when the traces within a pair are closer than 0.030 inches (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

4.3.2. Signal Isolation

The following are guidelines for signal isolation:

Figure 27Separate and group signals by function on separate layers if possible. Maintain a gap of 70 mils between all differential pairs (Phone-line and Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.03 inches away from any parallel signal traces.

Figure 28Physically group together all components associated with one clock trace to reduce trace length and radiation.

Figure 29Isolate I/O signals from high-speed signals to minimize cross-talk that can increase EMI emission and susceptibility to EMI from other signals.

Figure 30Avoid routing high-speed LAN or phone-line traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

4.3.3. Power and Ground Connections

The following are guidelines for power and ground connections:

Figure 31 All V_{CC} pins should be connected to the same power supply.

Figure 32 All V_{SS} pins should be connected to the same ground plane.

Figure 33 Four to six decoupling capacitors, including two 4.7 µF capacitors are recommended.

Figure 34 Place decoupling as close as possible to power pins.

The following are guidelines that will help reduce circuit inductance in both back planes and motherboards:

Figure 35 Route traces over a continuous plane with no interruptions (do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

Figure 36 Separate noisy digital grounds from analog grounds to reduce coupling.

Figure 37 Noisy digital grounds may affect sensitive DC subsystems.

Figure 38 All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.

Figure 39 Physically locate grounds between a signal path and its return. This will minimize the loop area.

Figure 40 Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics that can radiate EMI.

Figure 41 The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

Figure 42 Create a spark gap between pins 2 through 5 of the phone line connector(s) and shield ground of 1.5 mm (59.0 mil). This is a critical requirement needed to pass FCC part 68 testing for phone line connection.

Note: *For worldwide certification a trench of 2.5mm is required. In North America, the spacing requirement is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5mm spacing.*

4.3.4. A 4-Layer Board Design

Top Layer Routing: Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

Ground Plane: A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended.

Power Plane: Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDD_A. Analog power may be a metal fill “island,” separated from digital power, and better filtered than digital power.

Bottom Layer Routing: The digital high-speed signals that include all of the LAN interconnect interface signals are routed on the bottom layer.

4.3.5. Common Physical Layout Issues

This section lists common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair: Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair: (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ45/11 connector: Beyond a total distance of about 4 inches, it can become extremely difficult to design a specification-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below).
4. Routing any other trace parallel to and close to one of the differential traces: Cross-talk getting onto the receive channel will cause degraded long-cable BER. Cross-talk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inch from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces: The Transmit trace that is closest to one of the receive traces will put more cross-talk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. In the vicinities where the traces enter or exit the magnetics, the RJ45/11 and the PLC are the only possible exceptions.
6. Using an inferior magnetic module: The magnetic modules that Intel uses have been fully tested for IEEE PLC conformance, long-cable BER, and for emissions and immunity. (Inferior magnetic modules often have less common-mode rejection and/or no autotransformer in the transmit channel.)
7. Using an 82555 or 82558 physical layer schematic in a PLC design: The transmit terminations and decoupling are different, and there are also differences in the receive circuit.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ45/11 and for the wire-side center-taps of the magnetic modules: These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these unused pins are not terminated properly, emissions (FCC) problems, IEEE conformance issues, and long-cable noise (BER) problems can result.
9. Incorrect differential trace impedances: It is important to have ~100 ohms impedance *between* the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 ohms and 85 ohms, even when the designers think they have designed for 100 ohms. (To calculate differential impedance, many impedance calculators multiply only the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other (see NOTE below), the edge-coupling can lower the effective differential impedance by 5 ohms to 20 ohms. A 10-ohm to 15-ohm drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

Note: *It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to cross-talk and other sources of common-mode noise. Keeping them close means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. "Close" should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.*

10. Using a too-large capacitor between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetic) to ground: Using capacitors of more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that the signal fails the IEEE rise time and fall time specifications. This added capacitance can also cause return loss to fail at higher frequencies and will degrade the transmit BER performance.

Note: *Caution should be exercised if a capacitor is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) Unless there is some overshoot in 100 Mbps mode, these caps are not necessary.*

4.4. 82562EH HPNA Guidelines

This section provides more guidelines for implementing an 82562EH HPNA LAN connect component.

4.4.1. Power and Ground Connections

The following are guidelines for power and ground connections:

Figure 43For best performance, place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for 82562EH (V_{CCA}, V_{SSA}) should be isolated from the digital V_{CC} and V_{SS} through the use of ferrite beads. Also, adequate filtering and decoupling capacitors should be provided between V_{CC} and V_{SS}, and/or between V_{CCA} and V_{SSA} power supplies.

4.4.2. Guidelines for 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for placing components. Careful component placement can:

Figure 44Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.

Figure 45Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and cross-over between traces.

Minimizing the amount of space needed for the HPNA LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HPNA LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

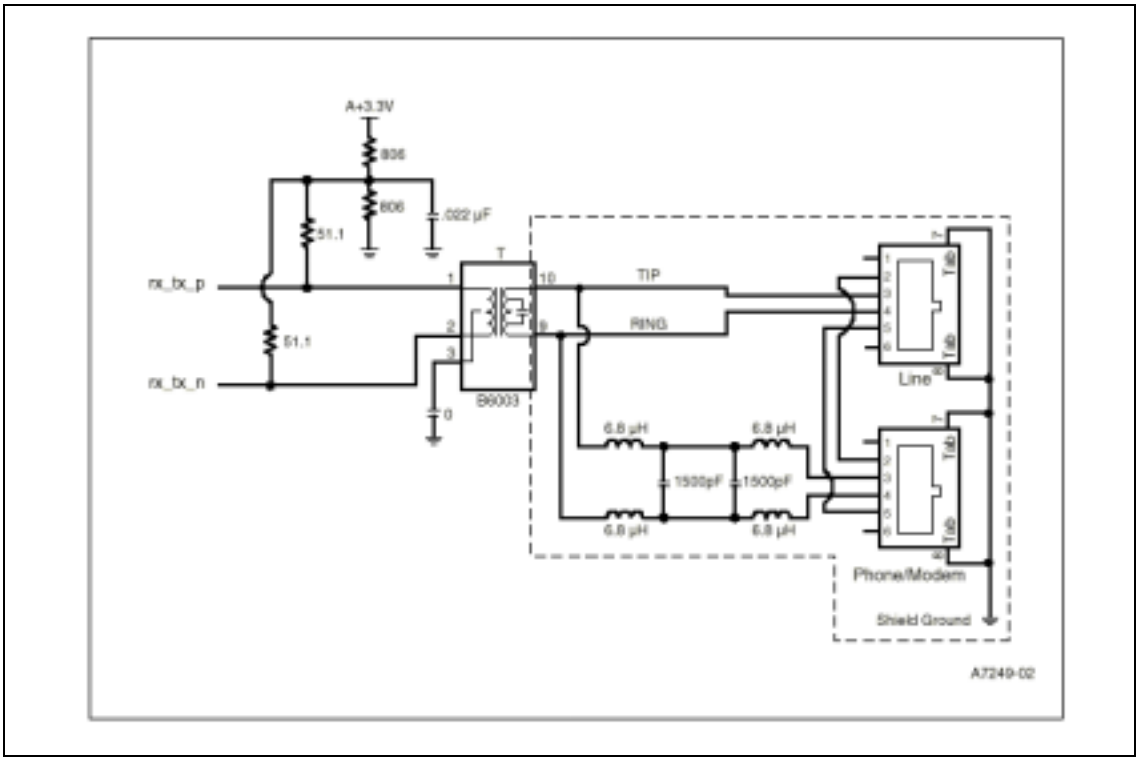
4.4.3. Crystals and Oscillators

To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HPNA magnetic module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possible radiation from the crystal case, and the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board. For noise-free and stable operation, place the crystal and associated discrete components as close as possible to 82562EH; keep the length as short as possible, and do not route any noisy signals in this area.

4.4.4. Phone Line HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1 Ω (1%) resistors. This parallel termination should be placed close to the 82562EH component. The center, common point between the 51.1 Ω resistors is connected to a voltage divider network. Figure 4-5 shows the termination.

Figure 4-5. 82562EH Termination



The filter and magnetic component T1 integrates the required filter network, high-voltage impulse protection, and transformer to support the HPNA LAN interface. One RJ11 jack (labeled “Line” in Figure 4-5 allows the node to be connected to the phone line, and the second jack (labeled “Phone/Modem” inFigure 4-5) allows other down-line devices to be connected at the same time. The second connector is not required by HPNA. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience. A low-pass filter, set up in-line with the second RJ11 jack, is also recommended by the HPNA to minimize interference between the HPNA connection and a POTs voice or modem connection on the second jack. This places a restriction on the type of devices connected to the second jack, because the pass-band of this filter is set at approximately 1.1 MHz.

Refer to the HPNA Web site for up-to-date information and recommendations about the use of this low-pass filter to meet HPNA certifications:

http://www.homepna.org/

5. Universal Serial Bus (USB)

5.1. USB Considerations on CNR Interface

There are two principal reasons to use USB on CNR:

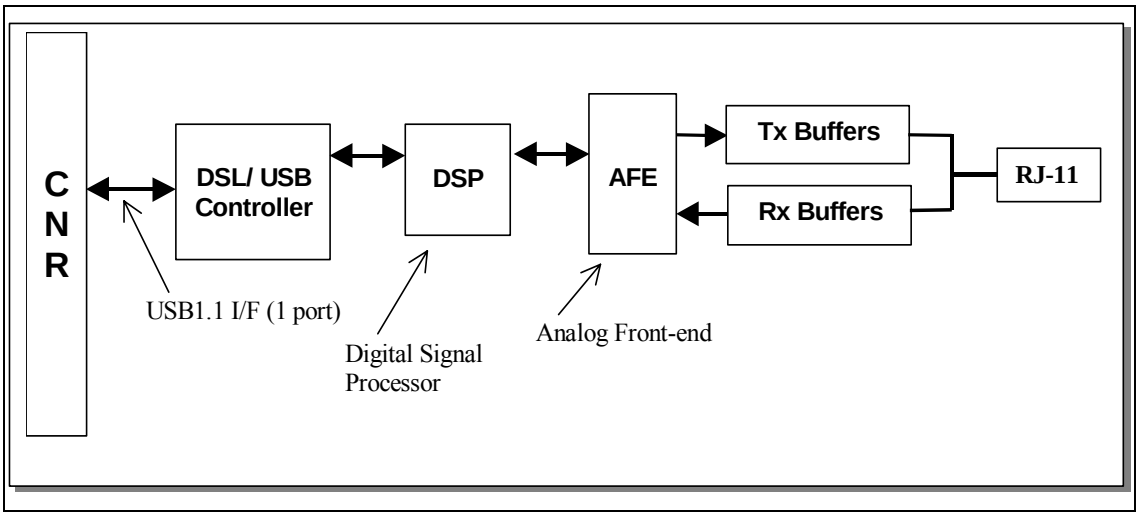
Figure 46USB can provide more USB ports to a system through the use of either a Hub device or a USB controller on the CNR card. Only one port can be routed to CNR, and this is specified as a low power port. System designers who want to add ports with high power capability will need to accommodate this on the CNR card.

Figure 47USB can be used to provide a host interface for other compatible technologies such as DSL or Wireless.

5.2. DSL and Wireless Implementations on CNR

Accommodating emerging technologies such as DSL and Wireless is part of the rationale for including USB on CNR. These technologies have not yet achieved an attach rate that justifies integration either in the chipset or discreetly onto the motherboard. In some geographic regions, however, the adoption of new technologies is accelerating. In the interim, a cost-effective solution is needed to give OEMs and system integrators the ability to address these regional markets. Figure 5-1 illustrates how USB can be used to provide a host interface for a DSL subsystem on a CNR card.

Figure 5-1. Example of USB/DSL Solution on CNR



It is possible to use the USB interface on CNR for designs such as the one above, or for other communications designs as well. These kinds of designs, using USB, are under development. Motherboard OEMs and system integrators should be aware that if USB is not routed to CNR, the motherboard will not support these types of CNR cards.

5.3. USB1.1 Design Consideration

CNR routes a single USB port from USB host controller to a CNR card. CNR is intended to support both USB 1.0/1.1 andg USB 2.0. The guidelines below are from the *Intel® 82801BA I/O Controller Hub 2 (ICH2) Design Guide*, Rev. 1.0, and are specific to that controller for USB 1.0 and/or USB 1.1 only.

Note: *Designers should be aware that the routing guidelines for USB 2.0 are different from these guidelines. Please refer to section 5.4 for the USB 2.0 routing considerations.*

General USB1.1 Design Considerations

Figure 48 Unused USB ports should be terminated with 15 K pull-down resistors on both P+/P- data lines.

Figure 49 15-ohm series resistors should be placed as close as possible to the Intel ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.

Figure 50 47-pF caps must be placed as close to the Intel ICH2 as possible and on the Intel ICH2 side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). These caps are intended to help signal quality (rise/fall time) and to help minimize EMI radiation.

Figure 51 15K +/-5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/- … P3+/-). The resistors are **required** for signal termination by the USB specification. The length of the stub should be as short as possible.

Figure 52 The trace impedance for the P0+/- … P3+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. Using the stack-up recommended in the Intel *ICH2 Design Guide,* Rev. 1.0 (Section 6.3), USB requires 9 mils traces. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.

Figure 53 USB data lines must be routed as critical signals. To minimize cross-talk, the P+/P- signal pair must be routed together and not parallel with other signal traces. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent cross-talk. There is no danger of cross-talk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length to minimize the effect of common mode current on EMI. Figure 5-2 illustrates the recommended USB data line implementation.

Figure 5-2. USB Data Signals

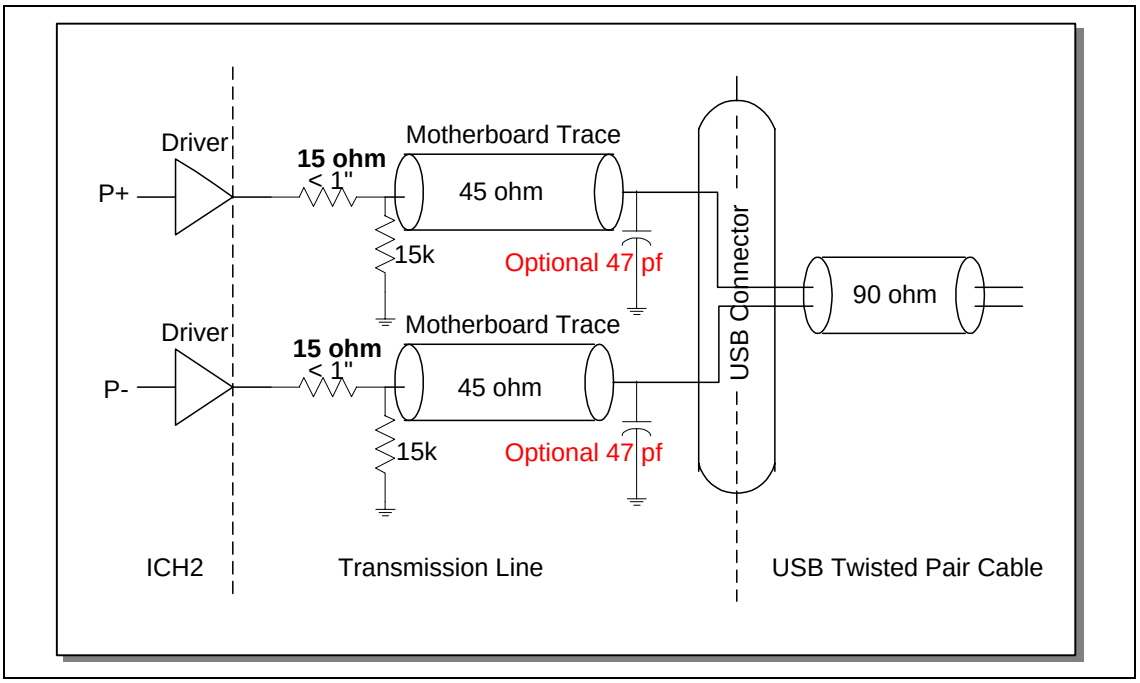


Table 5-1 specifies the recommended USB 1.1 trace characteristics.

Table 5-1. Recommended USB Trace Characteristics

Impedance Z0 = 45.4 Ω
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Resistance @ 20 °C = 53.9 mΩ

5.4. USB2.0 Design Consideration

CNR routes a single USB port from USB 2.0 Host Controller to a CNR card. CNR is intended to support both USB 1.0/1.1 and USB 2.0. The guidelines below are from the *USB 2.0 Platform Design Guideline*, Rev. 0.98, and are backward compatible to USB 1.0 and/or USB 1.1.

Note: *A whitepaper,"Implementation of USB2.0 on the Communication Networking Riser," will be available in early Q1'01 which will discuss the USB2.0 electrical and routing considerations on CNR in further detail.*

5.4.1. General USB2.0 Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. These recommendations focused on a four-layer motherboard and/or CNR card where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

Figure 54Place the USB 2.0 host controller and major components on the un-routed board first.

Figure 55With minimum trace lengths, route high-speed clock and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).

Figure 56Route USB 2.0 signals on bottom whenever possible.

Figure 57Route USB 2.0 signals using a minimum of via and corners. This reduces signal reflections and impedance changes.

Figure 58When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.

Figure 59Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.

Figure 60Stubs on USB 2.0 signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.

Figure 61Route all traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferrable to change layers to avoid crossing a plane split.

Figure 62Separate signal traces into similar categories and route similar signal traces together (such as, route differential pairs together).

Figure 63Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.

Figure 64Keep traces at least 50 mils away from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

5.4.2. USB 2.0 Trace Separation

The following considerations are based on a four-layer stack-Up

1. Signal 1 (top)
2. V_{CC}
3. GND
4. Signal 2 (bottom, best layer for USB2)

The specific board stack-up used is as follows:

Figure 651 ounce copper

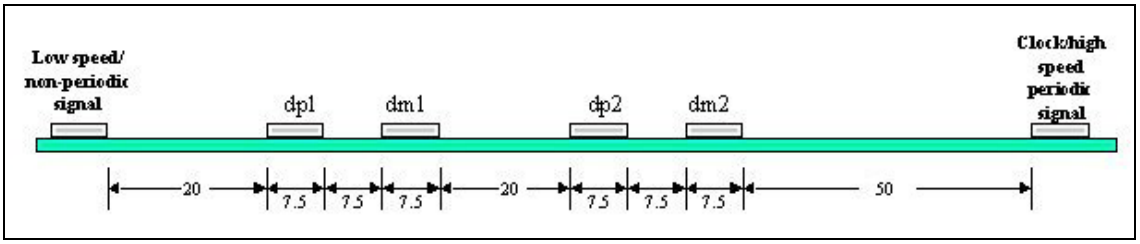
Figure 66pre-preg ≅ 4.5 mils

Figure 67core ≅ 53 mils

Figure 68board thickness ≅ 62 mils

Figure 69Dielectric constant $\varepsilon_r \cong 4.5$

Figure 5-3. Recommended Trace Spacing (mils) for the Stackup Given in Above



Use the following separation guidelines.

Figure 70Recommended trace width and separation is 7.5 mil trace with a 7.5 mil space.

Figure 71Maintain parallelism between USB 2.0 differential signals with the trace spacing needed to achieve 90 ohms differential impedance.

Figure 72Use a minimum 20 mil spacing between USB 2.0 signal pair and other traces on the PCB. This helps to prevent cross-talk. If possible, keep clock and PCI traces at least 50 mils from the USB differential pairs.

Figure 73Minimize the length of high-speed clock and periodic signal traces that run parallel to USB 2.0 signal lines to minimize cross-talk.

5.4.3. USB 2.0 Termination

Use the following termination guidelines.

Figure 74For downstream ports, a 15 kΩ pull down resistor on the connector side of the termination is required for device connection detection purposes. Note that this pulldown might be integrated into the host controller silicon. Follow the manufacturer's recommendation for the specific part used.

Figure 75A common mode (CM) choke should be used to terminate the USB 2.0 bus. Place the CM choke as close as possible to the connector pins.

5.4.4. USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 5-2. USB 2.0 Trace Length Guidelines

Configuration	Motherboard Trace Length	Cable Length	Front Panel Connector Card Trace Length	Maximum Length
CNR	**3-18”**	**NA**	**NA**	**18”**
Back Panel	3-18”	NA	NA	18”
Front panel	1-3”	(16” – Front Panel Connector Card Trace Length – Motherboard Trace Length)	1”	16”

— CNR numbers in this table are based on the following simulation assumptions
  — CNR configuration: max 6” trace on add-on card.

Note: *USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pairs (such as, DM1 and DP1) should be no greater than 150 mils.*

5.4.5. Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits, voids and cut-outs. Use the following guidelines for the V_{CC} plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks and signal traces as well as slower signal traces which might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode)
2. Avoid routing of USB signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

   When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

   If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high speed signal changes layers. As an example of bridging plane splits, a plane split that separates V_{CC5} and V_{CC3} planes should have a stitching cap placed near any high speed signal crossing. One side of the cap should tie to V_{CC5} and the other side should tie to V_{CC3}. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

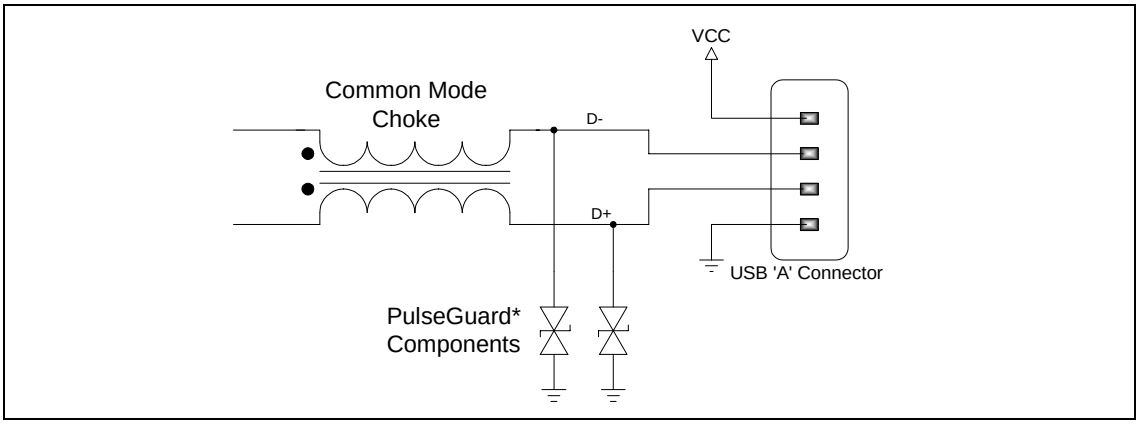
5.4.6. EMI/ESD Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

5.4.6.1. EMI - Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Figure 5-4 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

Figure 5-4. Common Mode Choke



Note: *Examples of specific common mode chokes that were tested for signal quality and EMI with passing results can be referenced in the USB 2.0 Platform Design Guideline, Rev. 1.0.*

Finding a common mode choke that meets the designer's needs is a two step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that the designer is trying to suppress.
2. Once the designer has a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality so be careful about increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low speed, Full speed and High speed USB operation.

5.4.6.2. ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of HS data. A device that has been tested successfully is based on spark gap technology. Proper placement of the device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 5-4 Other low-capacitance ESD protection devices may work as well but due to time and resource constraints none were investigated. As with the common mode choke solution, we recommend including the footprints for this device, or some other proven solution, as a stuffing option in case it is needed to pass ESD testing.

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6. System Management Bus (SMBus) and Plug and Play

The SMBus implements a simple interface to a serial EEPROM device on the CNR card. System BIOS reads the EEPROM at power-on, determines which CNR functions exist, and makes the appropriate entries in PCI configuration space. This ensures that the OS loads the correct drivers for each function.

6.1. Plug and Play EEPROM Registers

Table 6-1 lists the location and description of the registers that must be programmed to ensure correct PnP operation.

Table 6-1. Plug and Play EEPROM Registers

Word	Upper Byte	Lower Byte	Register Description
00	01	00	EEPROM ID
01	03	02	EEPROM Size
02	05	04	CNR Compliance
03	07	06	AC '97 Compliance
04	09	08	Function ID
05	0B	0A	Reserved Registers
06	0D	0C	Reserved Registers
07	0F	0E	Audio Pointer
08	11	10	Modem Pointer
09	13	12	USB Pointer
0A	15	14	SMBus Pointer
0B	17	16	LAN Pointer
0C	19	18	Reserved Registers
0D	1B	1A	Reserved Registers
0E	1D	1C	Reserved Registers
0F	1F	1E	Reserved Registers
10	21	20	Reserved Registers
11	23	22	Reserved Registers
12	25	24	Reserved Registers
13	27	26	Reserved Registers
14	29	28	Reserved Registers
15	2B	2A	Reserved Registers

Word	Upper Byte	Lower Byte	Register Description
16	2D	2C	Reserved Registers
17	2F	2E	Last Valid Address
18	31	30	Checksum
19	33	32	Modem Vendor ID
1A	35	34	Modem CNR Model ID
1B	37	36	USB Option Register
1C	39	38	LAN Option Register
1D	3B	3A	LAN CNR Vendor ID
1E	3D	3C	LAN CNR Model ID
1F	3F	3E	Reserved Registers
20-3F	—	—	Reserved Registers

7. CNR Power and Power Management Considerations

Table 7-1. CNR Electrical Specifications

Signal Name	Min.	Max.	Units	Comments
+5 Vdual/+5 VSB				
Tolerance	—	±5	%	Measured at the CNR connector
Ripple Voltage	—	0.075	V_{PK-PK}	Measured at the CNR connector
Supply Current				
Active State	—	0.500	Amps	ACPI S0 State
Wake enabled	—	0.500	Amps	ACPI S3 and S4 states
Not wake-enabled	—	0.020	Amps	ACPI S3 and S4 states
+3.3 Vdual				
Tolerance	—	±5	%	Measured at the CNR connector
Ripple Voltage	—	0.075	V_{PK-PK}	Measured at the CNR connector
Supply Current				
Active State	—	1.0	Amps	ACPI S0 state
Wake enabled	—	0.375	Amps	ACPI S3 and S4 states
Not wake-enabled	—	0.020	Amps	ACPI S3 and S4 states
CNR Total Power Dissipation	—	25	Watts	

7.1. CNR Interface Power Management

7.1.1. AC ’97 Interface Power Management

Table 7-2 defines the recommended power supplies for the AC ’97 interface (for audio and/or v.90 modem subsystems) on the CNR board.

Table 7-2. Recommended Power Distribution for the AC ’97 Interface Signals

	+Vmain[1]	+12 V/+5 VD[2]	-12 V	+Vdual[3]
AC-link (codec signals) BIT_CLK SDATA_IN	 ✓ (AC device) ✓ (AC device)			 ✓ (MC device, if primary) ✓ (MC device)
AC-link (controller signals) SYNC RESET SDATA_OUT	 ✓ (AC and MC devices) ✓ (AC device) ✓ (AC and MC devices)			 ✓ (MC device)
Riser digital logic	✓			
Modem analog circuitry		✓		
Modem wake logic				✓
Audio analog circuitry		✓	✓ (optional)	

—

— +Vmain refers to +3.3 VD or +5 VD.

— The selection of either the +12 V or the +5 VD for use in an analog system depends on the ultimate performance desired by the CNR designer. The +5 VD power supply is generally much noisier than the +12 V power supply.

— +Vdual refers to +3.3 Vdual or +5 V dual.

To enable wake from deep sleep modes, all CNR board-driven AC-link signals, as well as all other digital logic on the CNR board, must be powered by +Vdual. The +Vdual power supply must be used to power both the digital portion of the audio and/or v.90 modem codec and the AC-link portion of the digital controller, as specified in the *AC ’97 Specification*, Revision 2.1. It is recommended that the audio and/or v.90 modem subsystems locally regulate the +12 V down to +5 V analog for use by the subsystem's analog circuitry (to reduce signal degradation potentially introduced by the noisy digital power supply).

When the system enters a sleep state where the main power rails are shut off (that is, ACPI S3, or S4), those portions not related to wake-enabling (not connected to a standby power supply) will be completely shut off, consuming no power.

7.1.2. AMC ’97 Combination Codec CNR Board

The AMC ’97 combination codec CNR board must implement the same power distribution strategy as for the split-partitioned AC ’97-plus-MC ’97 CNR board. This leads to the possibility of an AMC ’97

codec design using split-power wells, thus enabling multi-voltage power distribution for different sections of the device.

7.1.3. LAN Interface Power Management

The CNR designer should refer to the appropriate data sheets for the LAN components to determine proper power supply connections to support an Instantly Available PC and "Off-yet Communicating" capabilities.

7.1.4. USB Interface Power Management and Interface Requirements

The USB interface section of the CNR connector consists of three signals and a power supply. The following sections describe the requirements for use of a USB interface on the CNR connector.

Note: *In addition to the statements in these sections, CNR designers must insure that their USB design complies with the Design Guidelines for the version of USB interface implemented on the CNR*

7.1.5. USB Differential Pair and Over Current Sensing

The CNR connector provides both the USB differential pair (USB+ and USB-) and the USB Over Current signal (USB_OC#). These signals are required to properly implement a USB device, function, or port on the CNR board. It is the responsibility of the CNR board designer to meet all of the USB specifications for the version of USB device, function, or port being implemented.

In addition to the requirements called out in the current version of the *Universal Serial Bus Specification*, the following requirements must also be met.

1. To minimize the possibility of USB speed-related failures, the design must meet the following three requirements.
   a. The CNR connector must be connected to the root hub on the motherboard.
   b. It is strongly recommended that the highest speed USB port on the motherboard be routed to the CNR connector.
   c. The CNR designer must insure that their USB design complies with the Design Guidelines for the version of USB interface implemented on the CNR.
2. If a USB device, function, or port is implemented on the CNR, the USB_OC# signal must be used to indicate if the device, function, or port attached to the USB+ and USB- signals has exceeded the maximum specified current (500 mA) by going low.
3. All USB port (15 kΩ) pull-down resistors must be located on the motherboard.
4. All USB function speed (1.5 kΩ) pull-up resistors must be located on the CNR board.

7.1.6. USB Power Management

Power for USB devices on the CNR can be provided through several of the supplies available on the CNR connector. However, if the USB device requires power while the system is in a sleep or suspended state, the +5 Vdual power supply must be used. Assuming that the +5 Vdual power supply is used to supply power to a wake-enabled USB device on the CNR, the requirements for the type of USB device are further defined, as follows:

1. If the USB signals on the CNR board are routed to a function (e.g., DSL v.90 modem), then the maximum current consumption must not exceed 500 mA on the +5 Vdual power supply in either an active system state or a wake-enabled system state.
2. If the USB signals on the CNR board are routed to a USB hub device, then the maximum current consumption must not exceed 500 mA in an active system state or a wake-enabled system state.
3. If a hub is placed on the CNR, no more than four ports from the hub can be used (either as externally available USB ports or functions on the CNR board).
4. If a hub is placed on the CNR, all devices or ports from the hub must be connected to low-power or self-powered USB devices or functions.

7.1.7. SMBus Interface Power Management

The power management for the SMBus interface is straightforward. The system must be in ACPI state S0, or a full working state, because the SMBus EEPROM (electrically erasable programmable read only memory) is accessed only at boot time by the BIOS. This implies that all power supplies are available. Thus, the SMBus EEPROM should be connected to the +3.3 VD power supply to ensure that it is functional only when the system is in a full working state.

7.2. Reset Considerations

The following sections describe the considerations for the AC ‘97 interface, when resetting/restoring the CNR board to a known state.

7.2.1. AC ’97 Interface Reset Considerations

The AC ’97 architecture defines three types of reset that AC ’97-compatible codecs must recognize:

Figure 76**Cold Reset**: Performs a complete codec hardware reset

Figure 77**Warm Reset**: Brings the AC-link out of PR4 low-power mode, no internal initialization required

Figure 78**Register Reset**: Reinitializes the codec through software command

In versions earlier than AC ’97 Version 2.1, when the PC is sleeping in either the ACPI S3, S4, or S5 states, and a wake-event occurs, the system brings the audio/v.90 modem subsystems back to full operation by reapplying power to the AC-link and asserting a cold-reset sequence.

AC ’97, Version 2.1, imposes a new requirement for AC-link RESET# behavior. This new requirement dictates that RESET# remain actively driven during S3, S4, or S5 states, so that auxiliary-powered v.90 modem codecs recognize, without doubt, that the AC-link RESET# was asserted, as opposed to floating at or near ground. Vdual-powered circuitry would then look for the trailing low-to-high transition on the AC-link RESET# signal, which indicates that the AC-link was powered back up and a “resume” reset sequence had occurred.

This presents an issue for v.90 modem codecs that are designed to wake the system from S3 or S4 states. An auxiliary-powered v.90 modem codec must retain portions of its internal state, including the wake-event state, after experiencing this resume sequence. The root issue is that the auxiliary-powered codec must be able to determine how to interpret and deal with the AC-link RESET# assertion so that the codec internal state is not corrupted when resuming.

There are numerous ways, ranging from hardware-only solutions to hardware/driver solutions, of addressing this without impacting either this specification or the *AC '97 Component Specification*. Providing any detailed implementation-specific information is beyond the scope of this specification.

7.3. AC '97 Clocking Considerations

7.3.1. AC '97 ACPI S0 "Working State" Clocking

In a multiple codec design, where audio is the primary codec (that is, the source of BIT_CLK), ACPI S0 working-state power management of the primary codec can present a clocking issue for the secondary codec.

For example, assume that the system is currently in the working state (ACPI S0) and the operating system power management policy manager determines that the audio (primary codec) is idle. At this time, the operating system may decide to transition the audio subsystem to its lowest power state (for example, D3hot). If the audio driver were then to place the audio codec down to its lowest power state (including PR4), the AC-link would enter its low-power mode with BIT_CLK stopped.

Had the v.90 modem been in use, or had it been needed at any time following this, it would be incapable of operating correctly because the audio driver had disabled its working state clock source (BIT_CLK).

For information on how this problem should be resolved, refer to the *AC '97 Component Specification*, Version 2.1.

Note: *The audio and v.90 modem drivers must be capable of operating completely independent of each other (for example, in the case when either the audio or v.90 modem hardware has entered a sleep state or has been disabled). All interdependencies (such as speakerphone audio and control) must be managed at the API level*

7.3.2. AC '97 ACPI S3 and S4 "Sleeping State" Clocking

An MC '97 (Modem/codec), when configured as the secondary codec, depends upon BIT_CLK from the primary codec for its normal, working-state clock source. When the system is in ACPI S3 or S4 sleep states the MC '97 must make provisions for a free-running clock source if needed for support of Caller ID capture or other wake-event related circuitry. This clock source must be powered by Vdual supply, and its frequency is recommended to be as low as is both economically and technologically possible to conserve power while the PC is asleep.

Note: *This applies to any state where the primary audio codec is not providing a free running BIT_CLK (i.e., BIT_CLK is held low or non-powered).*

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8. Windows Hardware Quality Lab (WHQL) Compliance Testing

This section is intended to help the designer anticipate issues that might arise while taking their products through the WHQL process. At the time of initial release of this publication, basic provisions for WHQL testing have been put in place. A Windows Logo for CNR cards is available under these provisions. It is important to understand, however, that the WHQL processes will evolve over time, and developers are encouraged to stay informed and participate in this evolution.

For direct contact with Microsoft WHQL about CNR logo testing, send e-mail to cnrhelp@microsoft.com. To subscribe to a weekly news e-mail that includes updates and changes made to the WHQL Web site, see instructions at http://www.microsoft.com/hwtest/news/.

8.1. Current WHQL Testing

Windows Logos can be obtained as follows:

1. Logo for a system shipped with CNR-capable motherboard **without** bundled CNR card. (Uses current system-level HCT kit.)
2. Logo for a system shipped with CNR-capable motherboard **with** bundled CNR card. (Each specific CNR card/motherboard combination *must* be tested. Uses current system *and device* HCT kits.)

The logos can be obtained by motherboard OEMs, system integrators or CNR card vendors. Vendors should test their configurations thoroughly, on their own, using the appropriate HCT kits before sending CNR card/motherboard combinations to Microsoft.

Note: *Specific CNR HCTs are being developed and will at some point augment the use of the existing HCTs in the CNR WHQL test process. The CNR tests will be ready at approximately the same time the Independent Motherboard Logo phase is started. (See Section 8.2.2.)*

8.2. Anticipated Evolution of WHQL Testing Process

It is expected that there will be four phases in the overall progression of CNR WHQL testing. These are outlined below:

Figure 79CNR Card/Motherboard Combination Logo (the test process mentioned above)

Figure 80Independent CNR Device Logo

Figure 81Independent CNR Motherboard Logo

Figure 82CNR Self-test Submissions

8.2.1. Independent CNR Device Logo

During the first phase of testing (CNR card/motherboard combinations), some motherboards will be identified as potential CNR card test references. Eventually some of these motherboards will be designated as test-reference motherboards. Once Microsoft has identified two or three reliable test-reference motherboards, the second phase of CNR testing can begin. This phase allows the independent testing of CNR cards using the test-reference motherboards.

Note: *For a motherboard to qualify as test-reference motherboard, it must perform reliably with all known validated CNR cards, and it must be readily available to the entire PC industry.*

Vendors seeking the CNR Device Logo should obtain all test-reference motherboards and use them to self-test their CNR card(s). The cards must be tested with all test-reference motherboards. After the vendor does self-testing, test logs are sent to Microsoft WHQL with the CNR cards. Microsoft repeats all testing to confirm the results. If the CNR card passes all tests, it will receive the CNR Device Logo.

8.2.2. Independent CNR Motherboard Logo

During the second phase of testing (Independent CNR Devices), some CNR cards will be identified as potential motherboard test-reference cards. Eventually some of these CNR cards will be designated as motherboard test-reference CNR cards.

The third phase of CNR testing can begin after Microsoft has identified some number of solid test reference CNR cards, and the specific CNR HCT kit has been released. This phase allows the independent testing of CNR-capable motherboards. This means that these motherboards may be Logo'd independent of any specific PC system or CNR card.

Note: *For a CNR card to qualify as a motherboard test reference, it must perform reliably with all test-reference motherboards, and it must be readily available to the entire PC industry*

Vendors seeking a CNR Motherboard Logo should obtain all test reference CNR cards and use them to self-test their motherboard(s). The motherboard must be tested with all test-reference CNR cards. After the vendor performs self-testing, test logs are sent to Microsoft WHQL with the motherboard. Microsoft repeats all testing to confirm the results. If the motherboard passes all tests, it will receive the CNR Motherboard Logo.

8.2.3. CNR Card Self-test Submissions

This is expected to be the final phase in the CNR WHQL test progression. This phase will begin at the discretion of Microsoft WHQL when they feel confident that any valid CNR card design will work reliably with any Logo'd CNR Motherboard.

The test process is essentially the same as the self-test processes detailed in the previous sections. Once the vendor completes the self-testing, the vendor submits the test logs to Microsoft WHQL. The vendor is not required to submit the CNR card for retesting by Microsoft. All CNR Card Self-test submissions must be made using the appropriate (or latest) version of CNR HCTs.

9. Related Documentation

The following documents were used as primary source material for the content of this design guide.

Figure 83*Communication and Networking Riser (CNR) Specification*, Revision 1.0

http://developer.intel.com/technology/cnr/

Figure 84*Audio Codec '97 Component Specificatio*n, Revision 2.1

Figure 85Intel ICH2 Design Guide, Revision 1.0

Figure 86Intel Recommendations for Intel ICHx/AC '97 Multichannel Audio (Intel White Paper)

Intel Restricted Documents:

Figure 8782562EH HomePNA 1 Mb/s Physical Layer Interface—Product Preview Datasheet OR-2015

*Figure 88*RS-82562EH 1Mb/s HomePNA LAN Connect Option Application Note OR-2065

Other related documents that can be found online:

Figure 89*Audio Codec '97 Component Specification*, Revision 2.1
http://developer.intel.com/ial/scalableplatforms/audio/index.htm

Figure 90Audio/Telephony Integration
http://developer.intel.com/ial/scalableplatforms/audio/doc.htm

Figure 91Hardware Acceleration and Redirection of Audio Streams
http://developer.intel.com/ial/scalableplatforms/audio/doc.htm

Figure 92AC '97 Controller/Codec/System Recommendations
http://developer.intel.com/ial/scalableplatforms/audio/doc.htm

Figure 93ACPI (Advanced Configuration and Power Interface) Specification
http://www.teleport.com/~acpi/

Figure 94*PCI Bus Power Management Interface Specification*, Revision 1.1
http://www.pcisig.com/

Figure 95Instantly Available PC Power Management Design Guide
http://developer.intel.com/design/power/pcpower.htm

Figure 96*Universal Serial Bus Specification*, Revision 1.1
http://www.usb.org/

Figure 97*System Management Bus Specification*, Revision 1.1
http://www.smbus.org/

Figure 98*PCI Local Bus Specification*, Revision 2.2
http://www.pcisig.com/

Figure 99*ATX Specification*, Version 2.03
http://www.teleport.com/~ffsupprt/

Figure 100*MicroATX Motherboard Interface Specification*, Version 1.0
http://www.teleport.com/~ffsupprt/

Figure 101*Accelerated Graphics Port (AGP) Specification*, Revision 2.0

http://www.intel.com/technology/agp/